[0103] Then, the gate interconnection formation step is performed as the step (S**100**). In this step (S**100**), for example, with the vapor deposition method, gate interconnection **70** composed of Al which is a conductor is formed to lie over potential fixing region **10**C. Then, in the present embodiment, gate interconnection **70** is formed to include gate interconnection extension portion **70**A extending beyond outer peripheral trench **22** to gate electrode **40**.

[0104] Then, the drain pad electrode formation step is performed as the step (S**110**). In this step (S**110**), as in the first embodiment, drain pad electrode **80** is formed to cover drain electrode **51**. By performing the steps (S**10**) to (S**110**) above, MOSFET **2** is manufactured and the semiconductor device manufacturing method according to the present embodiment is completed.

[0105] As described above, in MOSFETs **1**, **2** as the semiconductor devices according to the embodiments of the present invention above, active region **10**B and potential fixing region **10**C which is a semiconductor layer located outside active region **10**B are formed. Then, potential fixing region **10**C is electrically connected to source interconnection **60** arranged to lie over active region **10**B. Therefore, in MOSFETs **1**, **2** as the semiconductor devices according to the embodiments of the present invention above, a potential at the surface portion of the semiconductor layer located outside active region **10**B can be fixed to a potential as high as a potential of source interconnection **60**. Consequently, with MOSFETs **1**, **2** as the semiconductor devices according to the embodiments of the present invention above, the semiconductor device excellent in breakdown voltage characteristics can be provided.

[0106] In addition, with MOSFETs **1**, **2** as the semiconductor devices according to the embodiments of the present invention above, electrical connection between gate interconnection **70** arranged on potential fixing region **10**C and gate electrode **40** can readily be achieved while a potential of potential fixing region **10**C is fixed to a potential of source interconnection **60**. Then, MOSFETs **1**, **2** are different from each other in connection between potential fixing region **10**C and source interconnection **60** and connection between gate interconnection **70** and gate electrode **40**, as set forth below.

[0107] Initially, in MOSFET **1**, source interconnection **60** is electrically connected to potential fixing region **10**C without extending to potential fixing region **10**C. In addition, gate interconnection **70** is electrically connected to gate electrode **40** without extending to gate electrode **40**. Therefore, in MOSFET **1**, source interconnection **60** and gate interconnection **70** are readily arranged while a distance therebetween is maintained when viewed two-dimensionally. Consequently, according to MOSFET **1**, contact between source interconnection **60** and gate interconnection **70** can readily be avoided and short-circuiting between source interconnection **60** and gate interconnection **70** can be suppressed.

[0108] Meanwhile, in MOSFET **2**, potential fixing region **10**C is electrically connected to source interconnection **60** without extending to a portion below source interconnection **60**. Therefore, in electrical connection between potential fixing region **10**C and source interconnection **60**, potential fixing region **10**C can be formed more readily than in a case where potential fixing region **10**C is caused to extend to the portion below source interconnection **60**. In addition, gate electrode **40** is electrically connected to gate interconnection **70** without extending to a portion below gate interconnection **70**. Therefore, in electrical connection between gate electrode **40** and gate interconnection **70**, gate electrode **40** can be formed more readily than in a case where gate electrode **40** is caused to extend to the portion below gate interconnection **70**. Consequently, according to MOSFET **2**, a structure in semiconductor substrate **10** can be easier to form.

[0109] The semiconductor device and the semiconductor device manufacturing method according to the present invention can particularly advantageously be applied to a semiconductor device required to have a fixed potential at a surface portion of a semiconductor layer located outside an active region and a method of manufacturing the semiconductor device.

[0110] Although the present invention has been described and illustrated in detail, it is clearly understood that the same is by way of illustration and example only and is not to be taken by way of limitation, the scope of the present invention being interpreted by the terms of the appended claims.

1.-**6**. (canceled)

7. A method of manufacturing a semiconductor device, comprising the steps of:

preparing a semiconductor substrate including a drift layer having a first conductivity type and a body layer having a second conductivity type, which is formed on said drift layer to include one main surface;

forming a trench to open on a side of said one main surface and to penetrate said body layer and reach said drift layer;

forming a first insulating film to include a wall surface of said trench;

forming a gate electrode to be in contact with said first insulating film; and

forming a first interconnection on said one main surface,

in said step of forming a trench, an outer peripheral trench arranged to surround an active region when viewed two-dimensionally being formed, and

in said step of forming a first interconnection, said first interconnection being formed to lie over said active region when viewed two-dimensionally and to electrically be connected to a potential fixing region which is said body layer exposed at said one main surface opposite to said active region when viewed from said outer peripheral trench.

8. The method of manufacturing a semiconductor device according to claim **7**, wherein

in said step of forming a trench, said outer peripheral trench is formed simultaneously with said trench other than said outer peripheral trench.

9. The method of manufacturing a semiconductor device according to claim **7**, further comprising the step of forming an electric field relaxing region having the second conductivity type, which extends to be in contact with said outer peripheral trench in said drift layer and to reach said potential fixing region, wherein

in said step of forming an electric field relaxing region, said electric field relaxing region is formed through ion implantation.

10. The method of manufacturing a semiconductor device according to claim **7**, wherein

in said step of preparing a semiconductor substrate, a semiconductor substrate composed of silicon carbide is prepared.

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